MEMS-integrated VLSI Foundry Scheme in the University of Tokyo VDEC and its Applicability to Particle Sensor

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Introduction

Recent academic VLSI foundry and post-process opportunities for so-called "More-than-Moore" technology in Japan through the VLSI Design and Education Center (VDEC) is addressed.

General Instruction

One of the main axes of recent Very Large Scale Integrated Circuit (VLSI) research trend is process and device integration of MEMS (Micro Electro Mechanical Systems). Such technologies include VLSI post-processing by MEMS-originated fabrication technology (such as Deep Reactive Ion Etching) to provide MEMS-structure integrated monolithic devices. By such technology, together with sophisticated LSI design knowledge, brand-new high-performance sensor devices will become available. The VLSI Design and Education Center, the University of Tokyo, is developing a multi-user LSI fabrication foundry scheme on user-definable thick Silicon-on-Insulator (SOI) wafers. The fabricated SOI CMOS circuit is then post-processed in the participants' laboratories, including Takeda-Sentanchi Class #1 Supercleanroom, to produce integrated MEMS-VLSI system chip. The new VLSI foundry scheme and its applicability to high energy particle sensor will be addressed in the presentation.